[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the high speed implementation technique of image expanding equipment about image expanding equipment.
[0002]
[Description of the Prior Art] The so-called multimedia application which treats various data called not only a certain text but voice, an audio, a static image, and a dynamic image from recently and the former is becoming common. Since these multimedia data are huge, after they compress the amount of data into 1/hundreds from 1/dozens using the property which data once have, they are stored in external storage, such as a hard disk, or are transmitted through a network.
[0003] As a compression method For example, a dynamic image When making it an object, it is MPEG-1 (). [ISO/IEC] 11172 and "Information Technology-Coding of Moving Pictures and Associated Audio for Digital Storage Media upto 1.5 Mbits/s and "International Standards Organization/International Electrotechnical Commission, Geneva, and 1991 -- and MPEG-2 [more nearly quality than this MPEG-1] () [ISO/IEC] 13818, "Generic Coding of Moving Pictures and Associated Audio, "International Standards Organization/International Electrotechnical Commission, Geneva, and 1995 are known well.
[0004] the dynamic-image data compressed according to such MPEG specification -- the following -- "an MPEG bit stream" -- or it is only called a "bit stream." After an MPEG bit stream is stored or transmitted, it is elongated if needed (decoding) and the image of a decoding result is displayed.
[0005] Conventionally, although decoding of an MPEG bit stream was processed using Dedication LSI, it can come elongate the dynamic image compressed on microcomputer products, such as a personal computer and a home TV-game machine, according to MPEG specification using software with high-performance-izing of a general-purpose microprocessor (decoding).
[0006] A block diagram shows the outline of an example of the internal configuration of the microcomputer product which decodes an MPEG bit stream to drawing 13 . With reference to drawing 13 , the microprocessor 41 which performs decoding, the main memory 42 which stores the software for decoding and data, and I/O device 40 which performs the input of a bit stream 46 and the output of the decoding image 47 are connected with the internal bus 45.
[0007] The configuration of decoding of an MPEG bit stream is shown in drawing 14 . An MPEG bit stream takes a layered structure. The dynamic image of 1 relation is called a "sequence." A sequence is the assembly of "GOP (Group of Pictures)." GOP is the assembly of the still picture called the "picture" of two or more sheets (for example, 15 sheets). The picture of one sheet consists of two or more "slices", and one slice consists of "macro blocks" of 16 pixel x16 pixel. A macro block consists of 8 pixel x8 pixel "block" 4 pieces. Decoding is performed according to this hierarchy.
[0008] If drawing 14 is referred to, the decoding 121 of a sequence layer will be started after initialization 120. The decoding 121 of a sequence layer internally the decoding 122 of a GOP layer A call, The decoding 122 of a GOP layer internally the decoding 123 of a picture layer A call, The decoding 123 of a picture layer internally the decoding 124 of a slice layer A call, The decoding 124 of a slice layer calls the decoding 125 of a macro block layer, and the decoding 125 of a call and a macro block layer calls the decoding 126 of a block layer internally.
[0009] The working area for storing a decoding image is needed for decoding of an MPEG bit stream. Below, this working area is called a "frame buffer pool."
[0010] A frame buffer pool is secured as part of the initialization 120 of MPEG decoding software.
[0011] If the decoding 123 of a picture layer is started, a picture header unit will be decoded first, one frame buffer intact from a frame buffer pool next will be secured, and it will be used for decoding below a picture layer. If it becomes unnecessary after using the decoded picture for a display or a motion compensation, the frame buffer which stores the picture will be released.
[0012] An example of the configuration of a frame buffer pool is shown in drawing 15 . a frame buffer pool -- the frame buffers (a frame buffer 1, a frame buffer 2, --, frame buffers N and N are 8) 132, 133, and 134 of two or more sheets (N sheets), and the frame buffer management domain 130 -- since -- it becomes. The frame buffers 132, 133, and 134 of two or more sheets are placed on main memory 131. The frame buffer management domain 130 is also placed on main memory 131 in many cases.
[0013] The frame buffer of one sheet holds the picture of one sheet. The frame buffer management domain 130 has the entry of N individual corresponding to each frame buffer. Each entry holds the flag

135 which shows whether a corresponding frame buffer is "intact" or it is "under use", and the corresponding starting address 136 of a frame buffer.
[0014] Initialization of a frame buffer pool shall be completed at the time of initialization (120 of drawing 14) of MPEG decoding software. That is, at the time of decoding initiation of an MPEG bit stream, the frame buffers 132, 133, and 134 of N sheets are secured on main memory 131, the flag 135 of all the entries of the frame buffer management domain 130 is set as "intact", and the starting address 136 of all entries presupposes that the starting address of an effective frame buffer is held.
[0015] The processing flow of management of the frame buffer pool which showed the example of a configuration to drawing 15 is shown in drawing 16 as a flow chart.
[0016] In the decoding 123 (refer to drawing 14) of a picture layer, when securing a frame buffer, from the entry number 1 of the frame buffer management domain 130 to N is searched in ascending order, and the intact frame buffer discovered first is secured. That is, if the entry number for retrieval is set to i, it will set up with i= 1 first (step 141 of drawing 16).
[0017] And in investigating the flag 135 of the entry i of the frame buffer management domain 130 (step 142) and not being [be / it] "under use", it will use a frame buffer i (step 146), and when a flag 135 "is updated while in use" and is "under use", 1 is added and updated to Variable i (step 143), and the following entry is searched.
[0018] And if it investigated whether the value exceeded N (step 144) and the value of i is over N, after updating Variable i, since there will be no usable frame buffer, it considers as error termination (step 145).
[0019] Although retrieval sequence of the entry of the frame buffer management domain 130 is made into ascending order from the head entry, it may be searched with the example of a configuration shown in drawing 15 in descending order from a tail entry.
[0020]
[Problem(s) to be Solved by the Invention] About main memory 42, processing is accelerable by taking another configuration among the internal configurations of the microcomputer system which showed an example to drawing 13 . An example of the configuration for improvement in the speed is shown in drawing 4 for reference.
[0021] high-speed [as a component of main memory 42] with reference to drawing 4 -- but -- small -- although it is large capacity, a low speed dynamic RAM (memory 44 usually shows among drawing) can be considered to be a capacity static RAM (for high speed storage 43 to show among drawing).
[0022] Here, it becomes high cost although it is better to build main memory 42 using high speed storage 43 altogether if its attention is paid only to an engine-performance side. On the other hand, it becomes a low speed, although the cost per capacity usually built [that it is / the lower one / good] main memory 42 using memory 44 altogether when its attention was paid only to the cost side.
[0023] In the example shown in drawing 4 , memory 44 was usually combined with high speed storage 43, and comparatively high-speed main memory 42 is comparatively realized to low cost.
[0024] And in the system configuration shown in drawing 4 , comparatively high-speed processing can be performed on comparatively low cost main memory 42 system by usually putting another program and data on memory 44 for the program performed frequently or the data accessed frequently at high speed storage 43.
[0025] However, in the processing flow of the management method of the frame buffer pool shown in drawing 16 , the consideration to the main memory which combined such heterogeneous memory is not made, and it has the problem that the engine performance of the microcomputer system shown in drawing 4 cannot be demonstrated to the maximum extent.
[0026] Therefore, this invention is made in view of the above-mentioned trouble, and the purpose is in offering the equipment which realizes high-speed MPEG video decoder software on the microcomputer system which usually used together the memory and high speed storage like a static RAM like a dynamic RAM.
[0027]
[Means for Solving the Problem] It is characterized by what priority is given to the frame buffer which stores I picture and P picture which this invention is equipped with the memory system with which high-speed mold memory and ordinary type memory are intermingled in the equipment which elongates the bit stream compressed by MPEG specification, and are specified by MPEG on said high-speed mold

memory in order to attain said purpose, and is secured.
[0028] the frame buffer on [outline of invention] ordinary type memory -- adding -- a high-speed mold memory top -- one or more sheets -- (-- if it can do, the frame buffer of two or more sheet) will be secured, and it will assign with the priority to storing of I picture or P picture.
[0029] According to this invention, between the mean times of frame buffer access is shortened, and, thereby, the average activation engine performance of MPEG decoder software is raised because I and P picture with many counts of access increase the probability arranged on high speed storage since it is referred to at the time of motion compensation processing.
[0030]
[Embodiment of the Invention] The gestalt of desirable operation of this invention is explained below. This invention manages assignment of a frame buffer by the single frame buffer management domain (10 of drawing 1) in the gestalt of the desirable operation. The frame buffer (14 of drawing 1 , 15) on high speed storage (12 of drawing 1) is registered into a head part among the entries of a frame buffer management domain. The frame buffer (16 of drawing 1 , 17) on the usual memory (13 of drawing 1) of a low-speed mold is registered into the entry after these rather than high speed storage. (a) when securing the frame buffer which stores I picture and P picture It searchs in ascending order from the entry of the head of a frame buffer management domain, and when securing the frame buffer which stores (b) B picture, it searches in descending order from the entry of said last in a frame buffer management domain.
[0031] Since I and P picture with much access are given priority to and assigned by this to the frame buffer secured on high speed storage, the engine performance of MPEG video decoder software is improved.
[0032] Moreover, the frame buffer management domain where this invention manages assignment of the frame buffer on high speed storage for assignment of a frame buffer in the gestalt of the desirable operation (50 of drawing 5), Usually, it manages by the frame buffer management domain (51 of drawing 5) which manages assignment of the frame buffer on memory. (a) In order to secure the frame buffer which stores I and P picture The frame buffer management domain (50 of drawing 5) which manages assignment of the frame buffer on high speed storage previously Usually, the frame buffer management domain (51 of drawing 5) which manages assignment of the frame buffer on memory is searched behind. (b) In order to secure the frame buffer which stores B picture Usually, the frame buffer management domain (50 of drawing 5) which manages assignment of the frame buffer on high speed storage for the frame buffer management domain (51 of drawing 5) which manages assignment of the frame buffer on memory previously is searched behind.
[0033] Moreover, the frame buffer management domain which manages assignment of the frame buffer by which this invention assigns rate assignment of a frame buffer to I or P picture in the gestalt of the desirable operation (90 of drawing 9), It manages by the frame buffer management domain (91 of drawing 9) which manages assignment of the frame buffer assigned to B picture. The frame buffer which it secured at least one sheet at a time on high speed storage is registered into the head of the entry of both frame buffer management domains. (a) when securing the frame buffer which stores I picture or P picture The frame buffer management domain which manages assignment of the frame buffer assigned to I picture or P picture is searched in ascending order from an entry head. (b) The frame buffer which stores B picture searches the frame buffer management domain which manages assignment of the frame buffer assigned to B picture in ascending order from an entry head.
[0034]
[Example] The above-mentioned gestalt of operation is explained below with reference to a drawing about the example of this invention that it should explain to a detail further.
[0035] Below, the class of picture defined by MPEG and a mutual dependency are first explained as a premise. Next, three kinds are described about the configuration and its management flow chart of a frame buffer pool on the memory system which made high-speed smallness capacity memory and mass low-speed memory intermingled.
[0036] First, the class of picture defined by MPEG and a mutual dependency are explained. There are the three kinds of pictures defined by MPEG I, P, and B, according to the class of motion compensation.

[0037] In order not to use a motion compensation for decoding of I picture (Intra coded image; coded

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image in a frame), other frame buffers are not referred to at the time of decoding of I picture.
[0038] Forward prediction may be used for decoding of P picture (Predictive coded image; inter-frame forward direction predicting-coding image) among motion compensations. Therefore, at the time of decoding of P picture, I picture or one P picture decoded before may be referred to.
[0039] Bidirectional prediction may be used for decoding of B picture (Bidirectionally predictive coded image; both predicting-coding image) among motion compensations. Therefore, at the time of decoding of B picture, I picture or two P pictures which were decoded before may be referred to.
[0040] An example of the dependency according to picture class is shown in drawing 3 . Supposing it displays a frame 1 (I picture, 30), a frame 2 (B picture, 31), a frame 3 (B picture, 32), and a frame 4 (P picture, 33) in this sequence, the frame sequence on a bit stream will be a frame 1 (30), a frame 4 (33), a frame 2 (31), and a frame 3 (32), and will also perform decoding in this sequence.
[0041] A frame 1 (30) is decoded first. Since a frame 1 (30) is I picture, it is completed for frame 1 (30) itself, and don't refer to other frames for it for a motion compensation.
[0042] Next, a frame 4 (33) is decoded. A frame 4 (33) is P picture, and the motion compensation 36 by front motion prediction is performed, referring to the frame 1 (30) stored in the frame buffer at the time of decoding.
[0043] A frame 2 (31) is decoded to the 3rd. A frame 2 (31) is B picture, and the motion compensation 34 by bidirectional motion prediction is performed, referring to the frame 1 (30) and frame 4 (33) which were stored in the frame buffer at the time of decoding.
[0044] Finally a frame 3 (32) is decoded. A frame 3 (32) is B picture, and the motion compensation 35 by bidirectional motion prediction is performed, referring to the frame 1 (30) and frame 4 (33) which were stored in the frame buffer at the time of decoding.
[0045] Next, the configuration of the frame buffer pool on the main memory which made different-species memory intermingled is explained.
[0046] high-speed as main memory -- but -- small -- although it is capacity memory (static RAM [say / the following / "high speed storage"] 43) large capacity, with reference to drawing 4 which shows an example of a configuration of having combined low speed memory (dynamic RAM [say / the following / "it is usually memory"] 44), it explains below.
[0047] As a capacity of each memory, hundreds of K bytes (an example, 256-512 K bytes) of high speed storage 43 is considered that memory 44 is [several megabytes or more than it (an example, eight mega - 64 megabytes)] usually standard. The capacity of about 127 K bytes per one picture is required of resolution 354 pixels wide which is a standard picture format in MPEG-1, 240 pixels long, 8 bits of luminance signals, and a format called 8 bit two planes of every 4-pixel color-difference signals for every pixel. When following, for example, securing the frame buffer of eight sheets, all eight sheets cannot be secured from a limit of the capacity of high speed storage 43 on high speed storage 43. Therefore, at most 1 thru/or the frame buffer of two sheets are secured on high speed storage 43, and although the 7 remaining thru/or six sheets are low speeds, they will be secured on the cheap usual memory 44.
[0048] thus, the supervisory control approach of a frame buffer pool explained as the 1st to 3rd example below when both the frame buffer secured on high speed storage 43 and the frame buffer secured on the slow memory 44 exist -- two kinds of this frame buffer can be used properly, and the activation engine performance of MPEG decoding software can be improved. That is, by controlling to assign the frame buffer which gave priority to I accessed among three kinds of pictures contained in an MPEG bit stream at the time of decoding of a consecutiveness frame, and P frames over B frames which is not used for decoding of a consecutiveness frame, and secured them on high speed storage 43, a picture with many counts of access can be assigned with the priority to a high-speed frame buffer, and the execution speed of decoding software is accelerated.
[0049] The management method of the frame buffer pool concerning the 1st example of this invention is explained below with reference to drawing 1 and drawing 2 at a detail.
[0050] First, it has changed into the configuration which shows drawing 1 from the conventional method having shown the frame buffer pool in drawing 15 . That is, if drawing 1 is referred to, all the frame buffers (14 15) secured to ascending order on high speed storage 12 will be registered from 1 of the entry number of the frame buffer management domain 10, and the frame buffer (16 17) usually secured from these to the back entry (the example shown in drawing 1 the entry 3 or subsequent ones) on

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memory 13 will be registered.
[0051] The frame buffer management domain 10 has the entry of the number equal to the total frame buffer number N (sum total of the number of sheets of the frame buffer secured on high speed storage, and the number of sheets of the frame buffer usually secured on memory). Each entry holds the flag 18 which shows whether a corresponding frame buffer is intact or it is under use, and the starting address 19 of a frame buffer.
[0052] Initialization of the frame buffer pool shown in drawing 1 shall be completed at the 120 (refer to drawing 14) time of initialization of decoding software. That is, at the time of decoding initiation of an MPEG bit stream, the frame buffer of a total of N sheets is usually secured on memory 13, and the flag 18 of all the entries of the frame buffer management domain 10 is set as "intact", and makes the starting address 19 of all the entries of the frame buffer management domain 10 a high-speed-storage 12 top and the thing holding the starting address of an effective frame buffer.
[0053] The frame buffer pool shown in drawing 1 is managing by the approach shown below, and can attain improvement in the speed.
[0054] That is, when securing a frame buffer at the 123 (refer to drawing 14) time of decoding of a picture layer, the retrieval sequence of the entry of the frame buffer pool management domain 10 is changed with a picture type.
[0055] When securing the frame buffer for storing I or P picture, from the entry number 1 to N is searched in ascending order, and when securing the frame buffer for storing B picture, from the entry number N to 1 is searched in descending order. A picture type can be known if a picture header is decoded to the beginning of the decoding 123 (refer to drawing 14) of a picture layer.
[0056] Next, with reference to the flow chart of drawing 2 , the management method of the frame buffer pool shown in drawing 1 is explained in detail. Hereafter, the entry number for retrieval is set to i.
[0057] Judging the picture type stored in a frame buffer, (step 21) the procedure at the time of being I picture or P picture is as follows. First, it sets up with "1" as initial value of i (step 22).
[0058] If the flag of the entry i of the frame buffer pool management domain 10 is investigated (step 23) and it is not [be / it] "under use", a frame buffer i will be used, if the flag "is updated while in use" (step 27) and is [be / it] "under use", "1" will be added and updated to i (step 24), and the following entry will be searched. And since there will be no usable frame buffer if it investigated whether the value exceeded N (step 25) and i is over N after renewal of i, it considers as error termination (step 26).
[0059] Judging the picture type stored in a frame buffer, (step 21) the procedure at the time of being B picture is as follows.
[0060] First, "N" is set up as initial value of i (step 29). If the flag of the entry i of a frame buffer pool management domain is investigated (step 30), and it is not [be / it] "under use", and a frame buffer i will be used, a flag "will be updated while in use" (step 27) and it will become "during use", "1" will be subtracted and updated from i (step 31), and the following entry will be searched. Since there is no usable frame buffer when the value is investigated after renewal of i (step 32) and i becomes small from "1", it considers as error termination (step 33).
[0061] The frame buffer secured on high speed storage when securing the frame buffer for storing I with many counts of access and P picture according to the procedure shown in drawing 2 , as explained above is searched first, and when securing the frame buffer for storing B picture with few counts of access, the frame buffer previously secured on high speed storage in the frame buffer secured on the slow memory is searched behind. For this reason, according to this example, compared with the conventional method of securing a frame buffer, the execution speed of decoder software is accelerable irrespective of a picture type.
[0062] Although the frame buffer on high speed storage was registered into the head entry, I and the frame buffer for P pictures were searched in ascending order from the head entry and the frame buffer for B pictures was searched with the 1st frame buffer pool management method explained above in descending order from the tail entry, the same effectiveness is acquired, even if it registers the frame buffer on high speed storage into a tail entry, and searches I and the frame buffer for P pictures in descending order from a tail entry and searches the frame buffer for B pictures in descending order from a head entry.
[0063] Moreover, although the number of sheets of the frame buffer secured on high speed storage 12 considered as two sheets in the example shown in drawing 1 , the same argument as the above is

applicable about the number of sheets of the arbitration of one or more sheets.
[0064] Next, the 2nd example of this invention is explained. Drawing 5 is drawing showing the configuration of the 2nd example of this invention, and shows the configuration of the frame buffer pool which assigns a high-speed frame buffer to I and P picture preferentially. Moreover, it is a flow chart for drawing 8 to explain how to manage the frame buffer pool shown in drawing 5 , from drawing 6 .
[0065] Reference of drawing 5 has managed the frame buffer (55 56) secured on high speed storage 53, and the frame buffer (57 58) usually secured on memory 54 in this example in the respectively different frame buffer management domain (50 51).
[0066] The frame buffer of one N should be secured on high speed storage 53, and the frame buffer of two N shall usually be secured on memory 54. The frame buffer management domain is divided into the frame buffer management domain 1 with the entry of one N which manages the frame buffer on high speed storage 53 (50), and the frame buffer management domain 2 with the entry of two N which usually manages the frame buffer on memory 54 (51). Each entry of two frame buffer management domains holds whether a corresponding frame buffer is intact, the flag (501 511) which shows whether it is [be / it] under use, and the starting address (502 512) of a frame buffer.
[0067] Initialization of the frame buffer shown in drawing 5 shall be completed at the 120 (refer to drawing 14) time of initialization of decoding software. That is, at the time of decoding initiation of an MPEG bit stream, one N, the frame buffer of two N is usually secured on memory 54, the flag (501 511) of all the entries of the frame buffer management domain 1 (50) and the frame buffer management domain 2 (51) is set up intact on high speed storage 53, and the starting address (502 512) of all entries presupposes that the starting address of an effective frame buffer is held on.
[0068] Drawing 6 is the flow chart showing how to manage the frame buffer pool configuration shown in drawing 5 . When judging the picture type stored in a frame buffer with reference to drawing 6 (step 61) and securing the frame buffer for I and P picture, reservation of a frame buffer is first tried on high speed storage 53 (step 62).
[0069] At step 62, when a trial mistake of the reservation of a frame buffer is made on high speed storage 53, reservation of a frame buffer is usually tried on memory 54 (step 63). When it succeeds in either, it is normal termination (step 65), and it is error termination when all go wrong (step 64).
[0070] When securing the frame buffer for B picture, reservation of a frame buffer is usually first tried on memory 54 (step 66). When it goes wrong, reservation of a frame buffer is tried on high speed storage 53 (step 67). When it succeeds in either, it is normal termination (step 65), and it is error termination when all go wrong (step 68).
[0071] Drawing 7 is a flow chart for explaining the procedure which tries reservation for a frame buffer on high speed storage 53. Reference of drawing 7 initializes the entry number i for retrieval to "1" first (step 71). Next, the flag of the entry i of the frame buffer management domain 1 (50 of drawing 5) is investigated (step 72), if it is not [be / it] "under use", a frame buffer i will be secured, if the flag "is updated while in use" (step 76) and is "under use", "1" will be added and updated to i (step 73), and the following entry will be searched. When the value is investigated for i after updating (step 74) and i exceeds N1, since there is no frame buffer on usable high speed storage, it is taken as "secured failure" (step 75).
[0072] Drawing 8 is a flow chart for explaining the procedure which usually tries reservation for a frame buffer on memory 54. Reference of drawing 8 initializes the entry number i for retrieval to "1" first (step 81). Next, the flag of the entry i of the frame buffer management domain 2 (51 of drawing 5) is investigated (step 82), if it is not [be / it] "under use", a frame buffer i will be secured, if the flag "is updated while in use" and is (86) and "under use", "1" will be added and updated to i (step 83), and the following entry will be searched. When the value is investigated for i after updating (step 84) and i exceeds N2, since [being usable] there is no frame buffer on memory, it is usually taken as "secured failure" (step 85).
[0073] Also in the 2nd example explained above, at the time of the frame buffer reservation for I picture accessed frequently The availability of the frame buffer on high speed storage 53 (55 56) is searched preferentially. At the time of the frame buffer reservation for B picture Since the frame buffer (55 56) secured on high speed storage 53 is searched behind, compared with the conventional technique of securing a frame buffer, the execution speed of decoder software is accelerable irrespective of a picture type.

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[0074] In this 2nd example, the frame buffer management domain 1 (50) and the frame buffer management domain 2 (51) were searched in ascending order from the head entry as the flow chart showed to drawing 7 and drawing 8 , but even if it searches one of frame buffer management domains, or both frame buffer management domains in descending order from a tail entry, the same effectiveness is acquired.
[0075] Next, the 3rd example of this invention is explained. Drawing 9 is drawing showing the configuration of the 3rd example of this invention, and shows the configuration of the frame buffer pool which assigns a high-speed frame buffer to I and P picture preferentially. Moreover, drawing 10 and drawing 11 are the flow charts for explaining how to manage the frame buffer pool shown in drawing 9 . In addition, only on account of drawing creation, the part Fig. of drawing 10 and drawing 11 is carried out.
[0076] Reference of drawing 10 and drawing 11 has managed I, the frame buffer for P pictures, and the frame buffer for B pictures in another frame buffer pool management domain.
[0077] Suppose that the frame buffer of four N is secured for B pictures of three N I and for P pictures with the configuration shown in drawing 9 . However, suppose that one or more (preferably two or more sheets) sheets are secured on high speed storage, and the remainder is usually secured on memory among I and the frame buffer for P pictures. Suppose similarly that one or more sheets are secured on high speed storage, and the remainder is usually secured on memory among the frame buffers for B pictures.
[0078] A frame buffer management domain consists of the frame buffer management domain 3 with the entry of three N which manages I and the frame buffer for P pictures (90), and the frame buffer management domain 4 with the entry of four N which manages the frame buffer for B pictures (91). Each entry of both management domains holds the address (902 912) of whether a corresponding frame buffer is intact, and the flag (901 911) which shows whether it is [be / it] under use and initiation of a frame buffer.
[0079] Initialization of the frame buffer pool shown in drawing 9 shall be completed at the 120 (refer to drawing 14) time of initialization of decoding software. That is, at the time of decoding initiation of an MPEG bit stream, a high-speed-storage 93 top and a frame buffer usually required on memory 94 are secured, the flag (901 911) of all the entries of a frame buffer management domain (90 91) is set up intact, and the starting address (902 912) of all entries presupposes that the starting address of an effective frame buffer is held. Moreover, all the addresses of the frame buffer (95 96) secured to I and P pictures on high speed storage 93 are registered into ascending order from the entry 1 in the frame buffer management domain 3 (90). All the addresses of the frame buffer (97) similarly secured on the high speed storage 93 for B pictures are registered into ascending order from the entry 1 in the frame buffer management domain 4 (91).
[0080] Drawing 10 and drawing 11 are the flow charts showing the procedure of managing the frame buffer pool shown in drawing 9 . If drawing 10 is referred to, the picture type stored in a frame buffer is judged (step 111), and when securing the frame buffer for storing I or P picture, from the entry number 1 of the frame buffer management domain 3 (90) to N3 will be searched in ascending order.
[0081] First, the entry number i for retrieval is initialized to "1" (step 112). Next, if the flag of Entry i is investigated (step 113) and it is not [be / it] "under use", a frame buffer i will be used, if the flag "is updated while in use" (step 117) and is [be / it] "under use", "1" will be added and updated to i (step 114), and the following entry will be searched. Since there is no usable frame buffer when the value is investigated (step 115) and i exceeds "N3" after updating i, it considers as error termination (step 116).
[0082] When securing the frame buffer for storing B picture with reference to drawing 11 , from the entry number 1 of the frame buffer management domain 4 (91) to N4 is searched in ascending order. First, the entry number i for retrieval is initialized to "1" (step 119). Next, if the flag of Entry i is investigated (step 120) and it is not [be / it] "under use", a frame buffer i will be used, if the flag "is updated while in use" (step 124) and is [be / it] "under use", "1" will be added and updated to i (step 121), and the following entry will be searched. Since there is no usable frame buffer when the value is investigated for i after updating (step 122) and i exceeds "N4", it considers as error termination (step 123).
 [0083] According to the approach shown in drawing 10 and drawing 11 , the probability for the frame buffer secured to high-speed-storage top 93 to be assigned to the frame buffer on high speed storage 93 by the frame buffer pool for I or P pictures at I with many counts of access and P picture by 1

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and registering two sheets or more than it if it can do, usually giving priority over the frame buffer on memory 94, and searching is increased, and the execution speed of decoder software is accelerated. The frame buffer secured on the high speed storage 93 of at least one sheet is registered into the frame buffer pool for B pictures at coincidence, and the probability for decoding of B picture to be accelerated is increased by usually giving priority and searching from the frame buffer on memory 94.

[0084] Although many (an example, three sheets or more) frame buffers can secure comparatively the configuration of the 3rd example of the frame buffer pool explained above on high speed storage 93 and the usual processing can be performed on high speed storage 93, it is suitable for a system which usually secures more frame buffers on memory 94 in preparation for the worst case supposing fluctuation of a bit rate, or the load effect of tasks other than an MPEG software decoder.

[0085] Although there was three number of sheets of the frame buffer secured on high speed storage 93, and two sheets were registered into the frame buffer management domain 3 (90) and it registered one sheet into the frame buffer management domain 4 (91) inside with the configuration of the 3rd example of this invention shown in drawing 9 The frame buffer of two or more sheets is secured on high speed storage 93, and the same argument is applicable if one or more sheets are registered into the frame buffer management domain 3 (90) in one or more sheets and the frame buffer management domain 4 (91).

[0086] However, in the motion compensation which generates B picture, in order to perform bidirectional prediction with reference to the picture generated in the past of two sheets, it is desirable to secure the frame buffer of three or more sheets on the engine-performance top high speed storage 93, and to register two or more sheets into the frame buffer management domain 3 (90).

[0087] Memory 44 is usually connected with high speed storage 43 in an internal bus 45 at juxtaposition, and the configuration of the frame buffer pool explained in the 3rd example from the above 1st assumes the system which it is assigned on equal terms with the address space of a microprocessor 41, and is accessed, as shown in drawing 4 .

[0088] However, the configuration of the frame buffer pool explained in the 3rd example from the above 1st may be applicable also to the microcomputer system of a configuration of having been shown in drawing 12 .

[0089] With the configuration shown in drawing 12 , a static RAM is usually located between memory with a microprocessor, and is operating as cache memory 48. that is, the static RAM was usually used among the contents of memory recently -- the copy of some contents is held very much.

[0090] However, if the microprocessor is equipped with Cash Brock's lock device, replacement of a part of cache memory 48 can be forbidden, and it can use like the high speed storage 43 shown in drawing 4 . That is, the configuration of the 1st to 3rd above-mentioned frame buffer pool is applicable also to the microcomputer system shown in drawing 12 .

[0091] In addition, the processing explained with reference to the flow chart in the above-mentioned example is controlled by activation of the program instruction of a microcomputer.

[0092]

[Effect of the Invention] As explained above, according to this invention, the effectiveness that MPEG decoder software comparatively comparatively high-speed to low cost can be offered is done so using the system which combined the high speed storage and the mass usual memory of small capacity.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the image data decode approach and equipment. Especially this invention decodes the encoded input image data, stores this in memory per display, and in order to display this decode data, it relates to the approach and equipment which are read per display. This invention is applicable to an MPEG decoder as an example.
[0002]
[Description of the Prior Art] An image is compressed, it encodes and the technique stored in various storages, such as CD-ROM and DAT, is spreading so that it may be represented by the international coding standard MPEG. The home electronics maker and the computer maker are concentrating on development of a multimedia information appliance, and are aiming at commercial-scene installation of the goods based on MPEG today. Here, the processing in MPEG is outlined.
[0003] Drawing 1 is the mimetic diagram showing the flow of image coding and the decode by MPEG. The image inputted from the image input devices 2, such as a camera, is compressed and encoded by the video encoder 4 as shown in this drawing. Generally quantization processing and DCT (discrete cosine transform) are performed in the case of coding. The encoded data are written in a record medium 6.
[0004] Decode is this reverse, reads data from a record medium 6, and performs decode processing with the video decoder 8. After decode passes through reverse quantization processing and reverse DCT, it is performed. The image data decoded with the video decoder 8 is outputted to the format and timing which can be displayed, and is displayed and reproduced with a display 10. The forward direction prediction from a past playback image and the hard flow prediction from a future playback image, i.e., bidirectional prediction, are suitably used in the case of decode.
[0005] Drawing 2 is the block diagram of GOP (group OBU PIKUCHAZU) of MPEG. You may think that the screen (it is called a picture in MPEG) of 15 sheets shown in this drawing was photoed by this order. In MPEG, one prediction batch is formed by the picture of these [which are called GOP] 15 sheets. That is, it is designed so that coding and decode may be attained by the cross-reference of the picture in GOP, and GOP serves as a unit of random access. This sequence header of GOP and each GOP serves as a lot, and coding of a dynamic image and decode are attained by processing this group continuously.
[0006] As shown in this drawing, there are three kinds of pictures, I, P, and B. Coding closed within the self-frame is not performed and I picture (coded image in a frame) does not need reference of other pictures for decode. P picture (inter-frame forward direction predicting-coding image) is the object image of forward direction prediction, and the decode takes only a past playback image to it. On the other hand, B picture (bidirectional predicting-coding image) is the object image of bidirectional prediction, and I and P picture which come behind in order of playback are also referred to. In this drawing, the arrow head shows the prediction direction. Since it is necessary to know the contents of I inputted after B picture, or the P picture when actually encoding GOP, the point of B0 and B1 picture encodes and I2 picture is written in a record medium 6 as it is. In addition, the period M of I used for bidirectional prediction or P picture is 3 here.
[0007] Drawing 3 is drawing showing the sequence of the decode in MPEG, and playback. As for decode sequence and a lower train, the upper train of this drawing shows playback sequence. Decode

sequence is the same as coding sequence, and in agreement with the sequence that a picture is located in a line in a record medium 6. Therefore, in a decode side, from a record medium 6, after [I2 B3, and B4- -] reading a picture in order and decoding this, it returns in the original sequence and outputs. In this drawing, since I2 picture must not be outputted until it outputs B0 and B1 picture, it is held to the output of B0 and B1 picture at internal memory. Similarly, other I and P picture must be held in memory to the output of B picture related, respectively. Also in order not to enlarge capacity of memory, as shown in this drawing, B picture is outputted after decode as promptly as possible.

[0008] Drawing 4 is drawing showing decode and display-processing timing of the conventionally common video decoder 8. To the bottom of this drawing, the account of the average also of the picture held in a bank and each timing of the memory in the video decoder 8 on each bank is carried out. For the below-mentioned reason, this memory has four banks. Each bank is equivalent to the field which memorizes the data for one frame (one picture).

[0009] The period of frames 1-floor lines 6 is decided with a Vertical Synchronizing signal as shown in this drawing. Each frame period consists of two field periods, and for convenience, a field signal shows the first field period in a low, and it shows the second field period by the high.

[0010] In this drawing, the time of decode of I2, B0, and B1 picture already being completed is made into the origin of floor linel about a certain GOP. Therefore, subsequent decode continues with P5, B3, and B4-- as the decode sequence of drawing 3 . On the other hand, a display makes the time of only B0 picture being completed the origin of floor linel. Henceforth, it progresses with B1 and I2 -- as the playback sequence of drawing 3 . Hereafter, the decode and display in each frame period are explained.

[0011] (1) One Bfloor linel picture is displayed. For this reason, B1 picture is held till frame termination on the bank (it considers as bank 1 temporarily). I2 picture which should be displayed by floor line2 is held on another bank (it considers as bank 0). On the other hand, since P5 picture is decoded apart from a display, still more nearly another bank (it considers as bank 2) is assigned that this decode data should be stored. Decode is performed per macro block (1 macro block is the 16 pixel x length of 16 lines of width), and it is stored in memory in this unit. In addition, with this frame, bank 3 is a free area (intact).

[0012] (2) 2Ifloor line2 picture is displayed. I2 picture is held till frame termination on the bank 0. P5 picture which should be displayed later is held on bank 2. The data of B1 picture with which the display already ended are unnecessary, and are assigned to B3 picture whose bank 1 is the object of decode. Bank 3 is a free area also with this frame.

[0013] (3) Although the display of 3Ifloor line2 picture ended, this must be referred to now for B4 picture under decode, and continues being held on bank 0. B3 on display and P5 picture displayed later remain in a bank. B4 picture under decode is stored in the bank 3 per macro block. For this reason, four banks are needed for memory.

[0014] Henceforth, transition of drawing 4 is obtained according to the regulation of "displayed B picture is unnecessary" and "I and P picture being fixed period maintenance because of decode of B picture inserted into them." As shown in this drawing, all of four banks are used for every (floor lines 3 and 6, 9 --) three-frame period.

[0015]

[Problem(s) to be Solved by the Invention] As mentioned above, in the conventionally common video decoder 8, in order to hold, respectively, the memory of 4 banks was needed, until it decodes next B picture for the decoded picture, and until it actually displayed the picture concerned.

[0016] A capacity required in order to prepare these four banks in memory is explained. On the screen of 352 pixel x240 line of NTSC system, data of one frame are about 123.8 K bytes. In four frames, it becomes 495.2 K bytes. In MPEG, since it is desirable to prepare 40-50 K bytes of temporary buffer called a VBV buffer further, sum total capacity becomes about 540-550 K bytes. This runs short of capacity in one 4M bit DRAM in order to exceed 4M bit. On the other hand, in the PAL system of 352 pixel x288 line, data of one frame are about 148.5KB, and the same problem occurs too.

[0017] With the conventional video decoder 8, capacity is covered under such a situation by the approach of putting side by side 1M bit DRAM other than 4M bit DRAM. In order to correspond to the miniaturization of equipment, and low-pricing, though natural, it is desirable to realize this by one 4M bit DRAM. At this time, B picture which has not gone into memory every three frames should be thrown away, and the solution by the approach of **(ing) the picture displayed before one the first half of the 2nd inning should be avoided in the compromise on the specification which causes an image

quality fall, for example, the above-mentioned Prior art.
[0018] [Purpose] this invention is made in view of the above-mentioned technical problem, and the purpose is in offering the approach and equipment for using the memory of three banks in the aforementioned example, making evasion of an image quality fall a prerequisite. The description is in the point of performing read-out for a display, and the writing of decode data to the same memory bank by this invention for this purpose.
[0019]
[Means for Solving the Problem]
(1) The image data decode approach of this invention decodes the encoded input image data, stores this in each unit storing field of memory per display, and in order to display this decode data, it is related with the approach of reading per display. As for a "display unit", the picture of for example, one screen, a frame, and MPEG etc. says what constitutes the fixed unit in the case of a display here. The field where a "unit storing field" stores the data of this display unit is said. The storage region for one frame as used in the field of a frame memory is hit. In this invention, in order to realize the display which breaks off and which is not as a premise, it considers as what has the number fewer than the maximum number of the display unit which should be held in memory at coincidence of the unit storing fields prepared in memory. The condition of displaying certainly and smoothly in the sequence decided to be the display period which was able to decide the display unit to be "a display which breaks off, and which is not" is said. In the case of the above-mentioned conventional technique, "the maximum number of the display unit which should be held in memory at coincidence" is 4. Therefore, in the case of the same conditions as the conventional technique, this invention is applied when the number of the unit storing fields prepared in memory is three or less.
[0020] After decoding image data by this invention in this premise, if there is a vacant unit storing field, decode data are collectively stored in this per display. "-- bundling up -- " -- it is the semantics of **, without interrupting or standing by according to the situation of a display. On the other hand, when there was no vacant unit storing field, it stands by until read-out of decode data was started from one of unit storing fields for the display and read-out is performed to this field after decoding image data, finally storing of a display unit is ended by storing sequential decode data in the part which is vacant according to read-out. In this case, interruption may occur in storing actuation according to the situation of read-out.
[0021] (2) In a mode with the image data decode approach of this invention, said display unit is a frame. A frame is a concept containing the picture of MPEG. At this time, if this approach has a vacant unit storing field, it will start decode of the image data which should be decoded next to initiation and coincidence of a frame display period. On the other hand, if there is no vacant unit storing field, decode of the image data which should be decoded next will be predetermined-time-delayed from initiation of a frame display period, and it will start. In order to delay predetermined time, it is to perform read-out for a display from one of unit storing fields, and for an opening to arise.
[0022] (3) Moreover, in the mode which has this invention in this case, said input image data is encoded by the bidirectional predicting-coding use technique. There is MPEG in the example of a bidirectional predicting-coding use technique. At this time, when two or more frames for bidirectional prediction are inputted continuously, this invention predetermined-time-delays decode of the frame after the 2nd sheet from initiation of a frame display period, begins, and starts decode to initiation and coincidence of a frame display period about the other frame. The example of the frame for bidirectional prediction is B picture of MPEG, and reference of the frame after a self-frame (for example, I, P picture) is needed for decode of this frame for a display order. Therefore, the frame of the side referred to must be held in memory for a long time, and the situation that the opening of a unit storing field is lost easily arises. For this reason, decode is delayed and the opening produced to a field is used.
[0023] (4) In another mode of this invention, said display unit is a frame and this approach starts decode of the image data which should be decoded next regardless of the existence of a vacant unit storing field to initiation and coincidence of a frame display period. When there is no vacant unit storing field, sequential storing of the data decoded to the free area of the memory of the remainders other than a unit storing field is carried out. As an example of residual memory, there is a free space of the clearance between memory maps. While using residual memory, it waits for one of unit storing fields to be vacant.

[0024] (5) When it stands by until read-out of decode data was started from one of unit storing fields for the display when filled with the mode which has this invention in this case with the data which the free area of the memory of said remainder decoded, and read-out is performed to this field, carry out sequential storing of the remaining decode data at the part which is vacant according to read-out.
[0025] (6) In another mode of this invention, that by which input image data was encoded according to MPEG specification, and the period in which, as for said display unit, I or P picture appears as a picture and input image data are premised on 3 or more and the monograph affair of under capacity ** required for the capacity of memory to prepare four unit storing fields. When what was previously inputted among these pictures when B picture was continuously inputted in this situation (it is temporarily called a "point picture") is read from a unit storing field, sequential storing of the data of a picture (it is temporarily called a "back picture") later inputted into the part which is vacant according to read-out is carried out. At this time, the same unit storing field is temporarily shared with the data of two B pictures. Since it is not necessary to hold it if B picture is read, overwriting at the read part is allowed. For example, when 20% of a unit storing field is read, a back picture is overwritten by 20% of this part, and the 80 remaining% is still occupied by the point picture. Consequently, one unit storing field can be effectively used by two pictures.
[0026] (7) Contain an input means input the image data by which the image-data decode equipment of this invention was encoded with the bidirectional predicting-coding use technique on the other hand, a judgment means judge whether the inputted image data is data for bidirectional prediction, a decode means decode the inputted image data, a storing means store the decoded image data in memory, and the read-out means that read the image data which should display from memory to each frame display period. Said storing means stores data in the part which is vacant according to read-out one by one, when a free area does not exist in said memory in this configuration in the case of storing, the memory area where the data for bidirectional prediction are already stored is supervised and read-out is performed from this field.
[0027]
[Embodiment of the Invention] The operation gestalt of the image data decode equipment of this invention is explained here. The contents of the image data decode approach of this equipment to this invention also become clear.
[0028] Operation gestalt 1. drawing 5 is the whole image data decode equipment block diagram concerning the operation gestalt 1. With this drawing, decode processing is outlined first. With this operation gestalt, one 4M bit DRAM20 shall be used as memory which stores decode data. DRAM20 has three banks.
[0029] The class of picture etc. is discriminated from the reverse quantization section 10 which performs reverse quantization processing and reverse DCT processing to the coded image by which the ON force was carried out, respectively, the reverse DCT section 12, and the sequence header of the bit stream of a coded image. [Elements of the Invention] -- It is put on the latter part of the sequence Management Department 14 which offers a timing signal required for a motion compensation and DRAM control (after-mentioned), and a picture recognition signal, and the reverse DCT section 12. The address [as opposed to DRAM20 according to directions of the motion compensation section 16 which performs a motion compensation based on the motion vector used for the forward direction and hard flow prediction, and the motion compensation section 16], RAS/CAS etc. is generated and it has the DRAM control section 18 which controls the writing of decode data, and read-out of display TETA. As a result of a motion compensation, since a motion compensation is performed using the data read from DRAM20 while the contents and timing of access to DRAM20 become clear, the motion compensation section 16 and the DRAM control section 18 really have an indivisible relation on circuitry.
[0030] The DRAM bus 22 is a data bus on which the write-in data to DRAM20 and the read-out data from DRAM20 are once put. The video interface section 24 is connected to this bus, the indicative data read on the bus is incorporated, and it sends out to the video outlet section 26. The video outlet section 26 is outputted to the display which does not illustrate video signals Y (brightness), Cb (blue color difference), and Cr (red color difference). The description of this operation gestalt is in the sequence Management Department 14 which judges the continuation injection of B picture, and the DRAM control section 18 which stores sequential decode data in the unit storing field which is vacant gradually with read-out of an indicative data.

[0031] Drawing 7 is drawing showing the configuration which controls the timing of decode, when B picture continues among the DRAM control sections 18. When, as for "FIELD", the field signal of drawing 4 was supplied among this drawing and, as for "BB", B picture is supplied two or more continuation, continuous -- being active (yes) -- the becoming signal and the signal with which "DSTART" shows timing when decode initiation is most early possible -- The signal with which the signal, "VAD", and "DAD" "VEND" indicates the read-out completion timing of display (video) data to be show the address of a display and decode, respectively, and "DEC16" are the decode initiation indication signals for decoding in following the address which the display completed. Since a display and decode are performed per macro block, following decode is performed later than the displayed address by at least 16 lines. DSTART becomes active among continuous B pictures only in the first field of the 2nd sheet, and DEC16 becomes active similarly only in the second field so that it may mention later.

[0032] The frame signal-processing section 100 generates the first timing which starts following decode among this drawing. The frame signal-processing section 100 inputs FIELD, BB, DSTART, and VEND, and outputs a decode enabling signal and DEC16. The former is given to AND gate 108 and the latter is given to the address Monitoring Department 102. While following decode is continuing, the address Monitoring Department 102 compares VAD with DAD, and supervises both advance situation. The address Monitoring Department 102 starts monitor actuation by making DEC16 into a trigger. When decode is too quick as a result of a monitor, the low mask of said decode enabling signal is carried out by said AND gate 108. The decode enabling signal DECEN finally acquired is outputted from AND gate 108, and is referred to in a latter decode processing circuit (not shown).

[0033] When a [processing actuation] coded image is inputted, the class of this image is identified at the sequence Management Department 14. If an image is I picture, since it is possible, according to the usual procedure, decode completes this decode through reverse quantization, reverse DCT, and a motion compensation by reference of only the picture concerned. Decode data are stored in the empty bank of DRAM20 one after another per macro block. Since I picture is decoded by the beginning of GOP, the bank of DRAM20 is vacant and there is no trouble in storing of decode data in any way. It becomes the same processing also when an input image is P picture. It is because 3 is sufficient for a bank of DRAM20 also at the time of decode of P picture as shown in drawing 4 .

[0034] On the other hand, when an input image is B picture, situations differ. Originally four bank is required of the frame period 3 and floor lines 6 when the 2nd sheet of continuous B picture is decoded so that drawing 4 may show. Drawing 6 is drawing showing the decode and display-processing timing by this equipment. As shown in this drawing, the bank 1 is shared between this equipment by two B pictures in floor lines 3 and 6 (the following [floor lines / 3 and 6] frame display periods are called "share period"). Although the data for two frames cannot be held from the first with conventional equipment on one bank, the configuration shown in drawing 7 realizes this with this equipment. A timing chart explains this.

[0035] Drawing 8 is the timing-chart Fig. showing the situation of the following decode by the configuration of drawing 7 . In this drawing, it is three B picture FLn -n+2. It is shown. FLn It is B picture of the 2nd sheet and may be the 3 or 4th sheet henceforth. when, as for "VPASSD", the display address passes the decode address among this drawing, while the display address precedes with the decode address the pulse signal and "VLEADD" to which "DPASSV" becomes active, respectively when [that] reverse -- being active (yes) -- it is the becoming condition signal. VLEADD carries out toggle actuation by VPASSD and DPASSV. Moreover, with this operation gestalt, DECEN is generated as it is DEC16 and VLEADD or be alike as an example.

[0036] It sets to this drawing and is FLn first. It sets, and BB becomes active and DSTART becomes active once. Although decode is started by assertion and coincidence of DSTART in I and P picture, BB delays initiation of decode in floor line which became active to initiation of the second field with this operation gestalt. For this reason, DEC16 and DECEN become active from the second field (a points). Assertion of DEC16 is generated only in B picture of the 2nd sheet, and while DEC16 is active, a decoder circuit adjusts a decode rate and prepares the following decode condition of 16-line delay. That is, it realizes between DEC16 and following decode is FLn+1. It concentrates on maintenance of the following decode by the monitor of the address henceforth.

[0037] DEC16 is negated with negation of VEND (b points). DECEN is also negated here, decode stops

and only the display address progresses. If the display address goes around and the decode address is passed, VLEADD will become active and decode will be resumed (c points). DECEN is also negated, in order to have to reset and to have to consider the precedence condition of the display address, if the field changes (d points). Decode stops again now. Henceforth, VLEADD is decided by toggle actuation by the reset in a changing point, and VPASSD and DPASSV of the field, and DECEN is controlled by it.
[0038] The above is the approach of share period implementation using following decode. here -- being careful -- in order that decode initiation of B4 picture may be overdue, it is postponed until floor line4 by the completion of decode of the picture concerned. However, even in this case, since the head of a frame is performed in order, while displaying near a head, the remaining decode processing completes the display of B4 picture in floor line4, and a problem is not usually produced.
[0039] As mentioned above, although this operation gestalt explained focusing on the case (it is M= 3 at drawing 2) where B picture continues twice, even when continuing 3 times or more according to the equipment of this invention (M> 3), a bank of DRAM20 is good at 3. When B3, B4, B5, and B6 and a picture continue after I2 picture temporarily, bank 1 serves as a share period by two pictures of B3/B4, B4/B5, B5/B6, respectively after floor line3 of drawing 6 . That is, when the value of M increases, two or more share periods only continue, and it generates.
[0040] In addition, though natural, the equipment of this operation gestalt can be LSI-ized. In this case, how to form the reverse quantization section 10, the reverse DCT section 12, the sequence Management Department 14, the motion compensation section 16, and the DRAM control section 18 into 1 chip among drawing 5 can be considered.
[0041] With the operation gestalt 2. operation gestalt 1, decode initiation of next B picture was kept waiting to initiation of the second field in the share period. It is as above-mentioned that you may be postponed until floor line4 by completion of decode of B4 picture in floor line3 of drawing 6 , and, naturally there is a limitation also in this. With the operation gestalt 2, the equipment which starts decode from the first field also in a share period is indicated by using the memory area of the remainders other than three bank fields.
[0042] Drawing 9 is the memory map conceptual diagram of DRAM20 of the equipment of the operation gestalt 2. Although DRAM20 has banks 0-2 (respectively signs 30-32) and the VBV buffer 34 as shown in this drawing, the description of this operation gestalt is in the point of having the subbuffer 36 for decode data in addition to these. In addition, the field with which the minimum area usable as a subbuffer is not filled is drawn as a fraction field 38 (intact).
[0043] Since in the case of NTSC macro blocks gather 15 22 horizontal x length and constitute one frame, 22 lateral macro blocks are carried out to calling this a macro block line as 1 ** and **. At this time, one frame becomes the form where 15 macro block lines were accumulated. Drawing 10 is drawing showing the relation between one frame and a macro block line (it is written as "MBL" below), sets MBL to MBL 0 and 1 and --14 from a top, and is drawing MBL8 legible as an example in this drawing. Each MBL is equivalent to the length of 16 lines, and horizontal 16x22=352 pixel. The banks 0-2 of drawing 9 consist of 15MBL(s), respectively, they can deduct the VBV buffer 34 and the subbuffer 34 can carry out part grade reservation for 4MBL(s), when using 4 M bit DRAM. Here, this is explained as 4MBL(s).
[0044] With this operation gestalt, the condition that only B pictures are supplied in succession for explanation is assumed. Drawing 11 is the correspondence Fig. showing whether MBL 0-14 of B continuous pictures each is stored in a specific bank of DRAM20, and which MBL field of the subbuffer 34. Here, it is Bn. It is [the 1st sheet and] a picture henceforth Bn+1 It may be the 2nd sheet etc. When the continuation injection of the B picture is carried out, as shown in drawing 6 , since the bank shared is decided as one, it considers this as Bank A.
[0045] x of drawing 11 shows 15 MBL storing fields established in Bank A, and the number (physical address) of 0-14 is given. The number of 15-19 of a continuation is given to the subbuffer 34 as a physical address. In order to show that it is a physical address, PMBL [these] 0-19 is written.
[0046] On the other hand, y shows the picture decoded. The figures 0-14 in the lower column of each picture are the numbers of 15 MBL(s) which constitute the picture concerned, and this is equivalent to the logical address. Bi LMBLi [the logical address of a picture] 0-14 is written.
[0047] Decode of the equipment of this operation gestalt and a display action are explained.
[0048] It sets to drawing 11 and is Bn first. Decode of a picture is started. Bn The number of pictures is

the 1st and Bank A is vacant. Therefore, LMBLn 0-14 is stored in PMBL 0-14 as it is.
[0049] Continuously, it is Bn+1. Decode of a picture is started. Although decode was delayed to the second field with the operation gestalt 1, decode is immediately started from the first field like cases, such as I picture, with this operation gestalt. LMBLn+1 0-3 equivalent to head 4MBL of decode data are stored in PMBL 15-19 of the vacant subbuffer 34. For this reason, it is not necessary to wait for read-out from Bank A.
[0050] On the other hand, it is Bn also between this storing. Read-out for the display of a picture is performed in parallel. Since it is thought that read-out of LMBLn 0 at least will be completed by the time storing to PMBL 15-19 is completed, LMBLn+1 4 are overwritten PMBL0. What is necessary is just to stand by, if read-out of LMBLn 0 is not completed. Henceforth, it is Bn+1, supervising like the operation gestalt 1, so that decode may not pass a display. Decode and storing of a picture are performed.
[0051] Next, it is Bn+2. It progresses to decode of a picture. It is Bn+1 as shown in this drawing. Since even PMBL10 is used by the picture, LMBLn+2 0 is stored from PMBL11. Decode initiation timing can be brought forward by storing decode data cyclically similarly hereafter from the place as for which PMBL 0-19 is vacant. Consequently, according to this operation gestalt, even if the picture which needs long decode time amount comes, sufficient decode time amount is securable.
[0052]
[Effect of the Invention] According to the image data decode approach and equipment of this invention, decode of a good image and a display are attained with the number of banks with which the number of banks of memory required for decode and a display originally is not filled. Consequently, the capacity of memory can be reduced compared with the former and it contributes to a miniaturization and cost cut of equipment. Moreover, it is not necessary to perform curtailment on a specification which causes an image quality fall at this time. When using the memory area of the remainders other than a bank effectively, it can contribute to reservation of decode time amount.

[Translation done.]